Abstract

A method and circuit for improving linearity of a folding or flash analog-digital-converter (ADC) circuit. Averaging resistors connect outputs of each of a bank of first pre-amplifiers. A series adjustment resistor is placed between each node connecting the output of a first bank pre-amplifier and the associated averaging resistor, and the input of each of a second bank pre-amplifier. An adjustment current is injected through the adjustment resistor during a calibration. A permanent value for adjustment current is determined such that an effect of offset errors is substantially minimized.